Claims

[c1] What is claimed is:

1.A single-poly EEPROM, comprising:

a first PMOS transistor serially connected to a second PMOS transistor, wherein the first and second PMOS transistors are both formed on an N-well of a P-type substrate, and whereinthe first PMOS transistor includes a floating gate, a first P^+ doped drain region, and a first P^+ doped source region, the second PMOS transistor includes a gate and second P^+ doped source region, and the first P^+ doped source region of the first PMOS transistor serves as a drain of the second PMOS transistor; and

an erase gate formed in the P-type substrate in the vicinity of the first PMOS transistor, wherein the floating gate of the first PMOS transistor overlaps with the N-well and the P-type substrate and extends to the erase gate.

[c2] 2.The single-poly EEPROM of claim 1 wherein the erase gate is an N-type doped region formed in the P-type substrate beneath the floating gate.

[c3] 3.The single-poly EEPROM of claim 2 wherein the N-type doped region substantially does not overlap with the floating gate.

[c4] 4.The single-poly EEPROM of claim 2 further comprising a floating gate oxide layer between the erase gate and the floating gate.

[c5] 5.The single-poly EEPROM of claim 1 wherein when applying a pre-selected drain bias (V_d) to the second PMOS transistor, the floating gate of the first PMOS transistor obtains an induced voltage due to capacitance coupling effects, thereby turning on a P-channel under the second PMOS transistor and obtaining a gate current near a maximum value.

[c6] 6.The single-poly EEPROM of claim 5 wherein V_d is about 5V.

[c7] 7.The single-poly EEPROM of claim 1 wherein the first PMOS transistor is a single-gate transistor without any control gate formed above the floating gate of the first PMOS transistor.

[c8] 8.The single-poly EEPROM of claim 1 wherein when operating the single-poly

EEPROM, a pre-selected erase gate bias and a first doped drain region voltage are applied to the erase gate and the first doped drain region so as to pull trapped electrons out of the floating gate by way of tunneling.

[c9] 9.The operation of single-poly EEPROM as set forth in claim 8 wherein phenomenon of over-erasing is avoided.

[c10] 10.The single-poly EEPROM of claim 8 wherein pre-selected erase gate bias is positive, and the first doped drain region voltage is negative.